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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/783,712	02/20/2004	Orazio Musumeci	851763.448	5607

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EXAMINER	
PATEL, NIMESH G	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 10/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/783,712	MUSUMECI ET AL.	
	Examiner	Art Unit	
	Nimesh G. Patel	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *20040714*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Catherwood(US 20020194466), in view of Chiu(US 6401154).

3. Regarding claim 1, Catherwood discloses a microcontroller device, comprising: a control unit, the control unit having a plurality of logic modules including a processing module for executing processing procedures; an interrupt managing module for managing program interruptions caused by internal or external events(Figure 1; Paragraph 9); and a set of interruption registers associated with said control unit for storing information regarding interrupts(Figure 1; Paragraph 53) and for requesting arrest of said processing module for executing processing procedures(Paragraph 57).

Catherwood does not specifically disclose an arbiter module for managing switching of said plurality of modules. However, Chiu discloses an arbiter module for managing switching of plurality of modules(Figure 1, 68). Therefore it would have been obvious to one of ordinary skill in the art to include an arbiter module, as disclosed by Chiu, in the system of Catherwood for arbitrating between the plurality of modules to use a common shared bus.

4. Regarding claim 2, Catherwood discloses a microcontroller device, wherein said set of interruption registers comprises: a register of the served interrupts; a register containing the information regarding which interrupt has interrupted execution of the processing procedure;

and a register in which there is stored the state of the module for managing the processing procedure at which said interrupt has occurred(Paragraphs 61-62; Figure 5, 530-560).

5. Regarding claim 3, Catherwood discloses a microcontroller device, wherein the control unit writes said information directly in said interrupt registers and sends a selection signal containing information on the interrupt served(Figure 5; Paragraphs 61-62).

6. Regarding claim 4, Catherwood discloses a microcontroller device, wherein downstream of the register of the served interrupts and of the register containing the information regarding which interrupt has interrupted execution of the processing procedure, there are provided respective multiplexers driven by said selection signal, and in that the outputs of said multiplexers are sent at input to a logic gate to obtain a return selection signal(Paragraphs 61-62).

7. Regarding claim 5, Catherwood and Chiu do not specifically disclose a microcontroller device, wherein said plurality of logic modules comprises finite state machines. However, finite state machines are well known in the art and it would have been obvious to one of ordinary skilled in the art to be able to implement the modules of Catherwood and Chiu in the form of finite state machines.

8. Regarding claim 6, Catherwood discloses a microcontroller device, wherein said processing module is configured for executing iterative processing procedures(Paragraph 9).

9. Regarding claim 7, Catherwood discloses a method for managing the program interrupts in a microcontroller device, which provides for the using of a module for managing the executive processing procedure of a control unit belonging to said microcontroller device for executing processing procedures and provides for managing interrupts by means of an interrupt managing module(Paragraph 9), the method comprising the following operations: upon occurrence of an interrupt in a state of the processing procedure, transferring the control from the module for

managing the executive processing procedure to the interrupt managing module(Paragraph 56); storing the information regarding the interrupt that has occurred in interrupt registers(Paragraph 53); at the end of the interrupt, transferring control to the interrupt managing module for execution of an instruction of a "return from interrupt" type; and restoring the control to the module for managing the processing procedure at the state in which the interrupt occurred(Paragraph 57).

10. Regarding claim 8, Catherwood discloses a method, including the operations of: evaluating whether the interrupt has occurred at a standard instruction; and in the negative, restoring the control to the module for managing the processing procedure at the state where the interruption occurred; and in the positive, restoring the control to an arbiter module(Paragraphs 61-62).

11. Regarding claim 9, Catherwood discloses a method, wherein said operations of restoring the control to an arbiter module take place under the control of a return selection signal obtained from the information regarding the interrupt that has occurred stored in the interrupt registers(Paragraphs 61-62).

12. Regarding claim 10, Catherwood discloses a method, wherein the information regarding the interrupt that has occurred and which is stored in the interrupt registers comprises information regarding the interrupt served, information regarding the interrupt that has occurred during the processing procedure, and the state of the processing procedure in which the interrupt that has occurred(Paragraphs 61-62; Figure 5, 530-560).

13. Regarding claim 11, Catherwood discloses a method, comprising the operation of configuring said processing module for execution of iterative processing procedures(Paragraph 9).

14. Regarding claims 12-21, Catherwood and Chui disclose a microcontroller device and method for operating the microcontroller device since they describe the invention of claims 1-11, which are rejected for the reasoning above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nimesh G. Patel whose telephone number is 571-272-3640. The examiner can normally be reached on M-F, 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Nimesh G Patel
Examiner
Art Unit 2112

NP
September 30, 2006

MARK H. RINEHART
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